ABSTRACT

In accordance with the objectives of the invention a new method is provided for testing DRAM cells using a slow-speed tester. An adjustable self-time scheme is provided that is used for write-recovery during the testing of DRAM devices using a low-speed tester. CSL and WL pulses are self-time controlled and are in this manner used to emulate DRAM operation under different operational conditions. The adjustable self-time scheme of the invention can be used to screen write recovery (twr) depending on field requirements for the DRAM cell, a low-speed tester can be used for the screening.